

106280-05221260

FIG.2

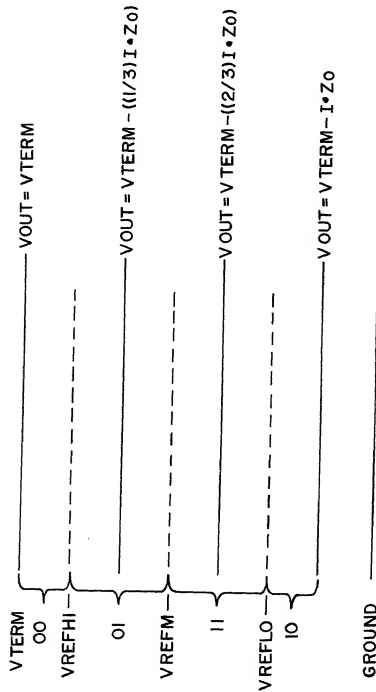


FIG.3A

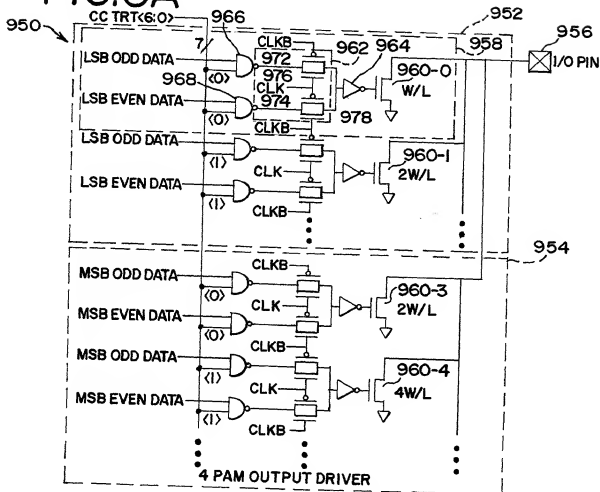


FIG.3B

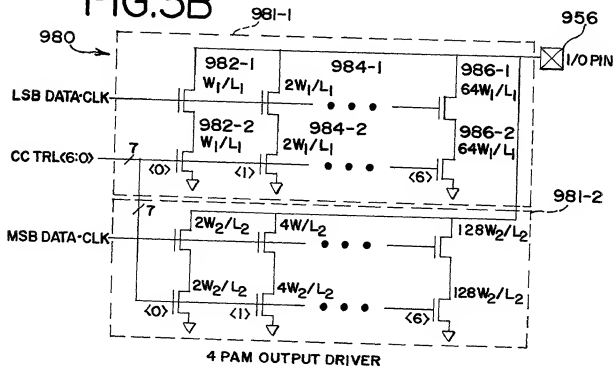


FIG. 4A

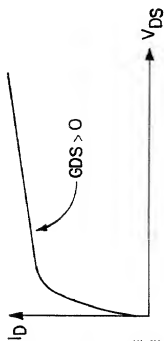


FIG. 4B

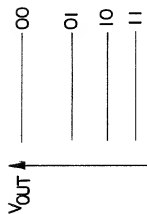


FIG. 4C

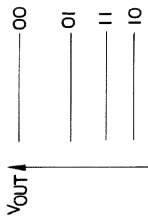


FIG.5B

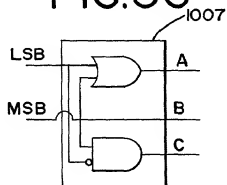
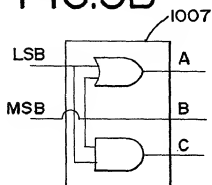
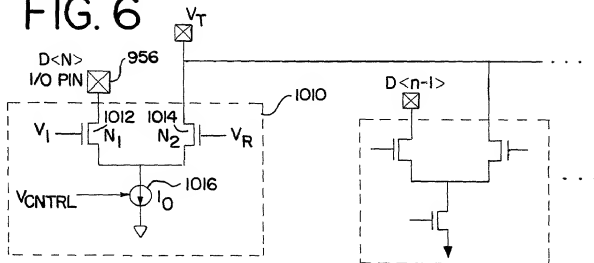


FIG. 6



CIRCUIT TO REDUCE SWITCHING NOISE

FIG. 7

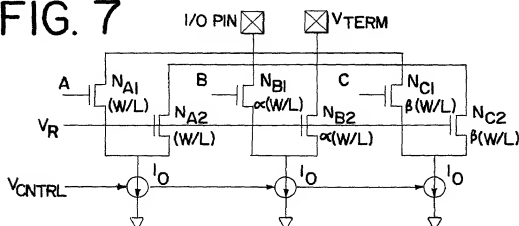
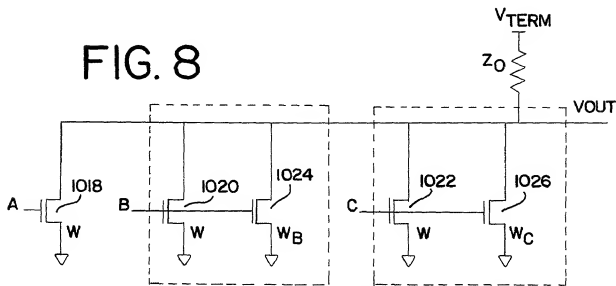
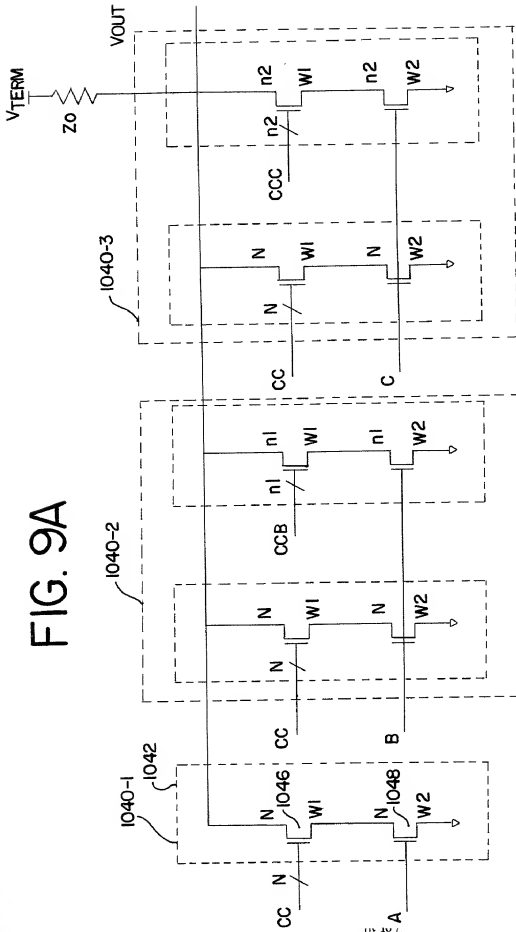


FIG. 8



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER

FIG. 9A



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 9B

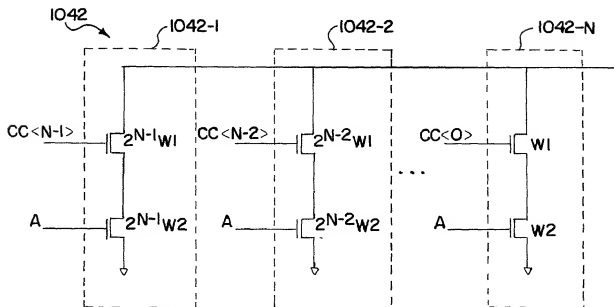
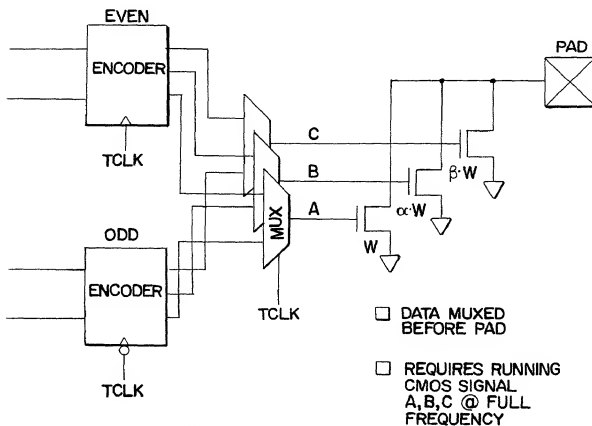
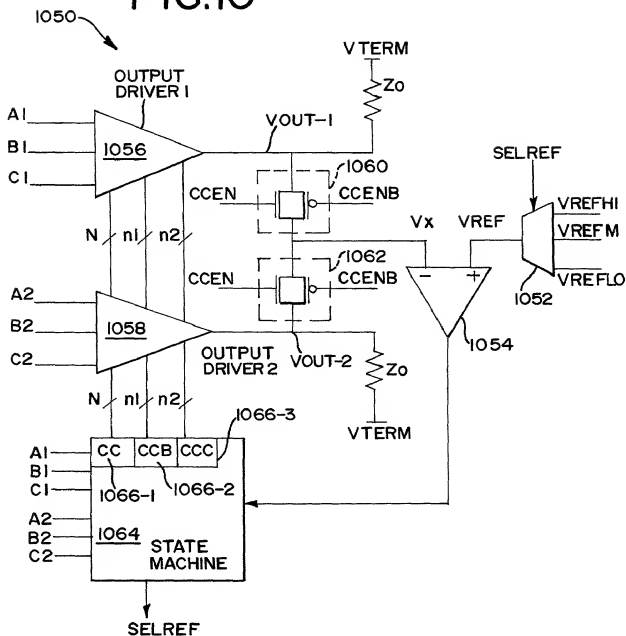


FIG. 9C



09742250.082301

FIG.10



CIRCUIT FOR CALIBRATING THE GDS COMPENSATED
 OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11A

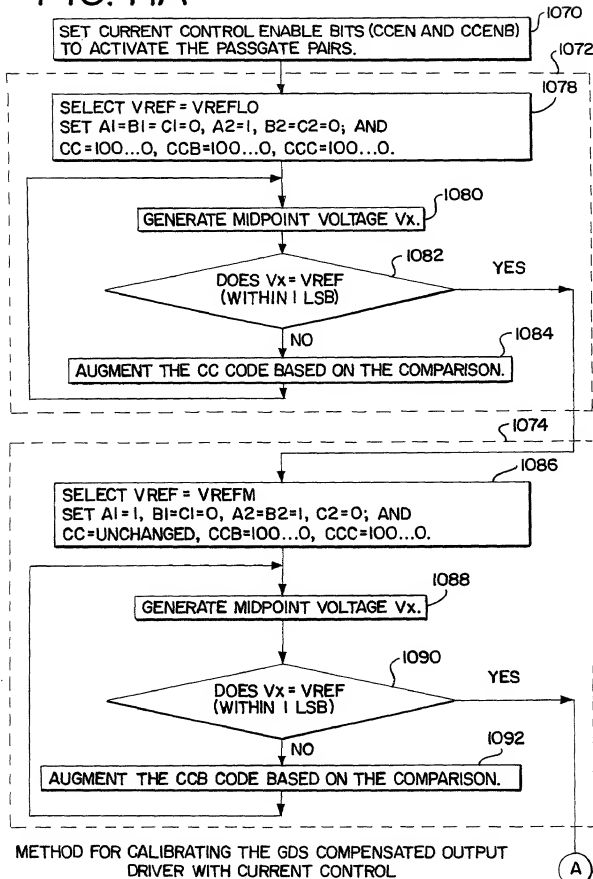
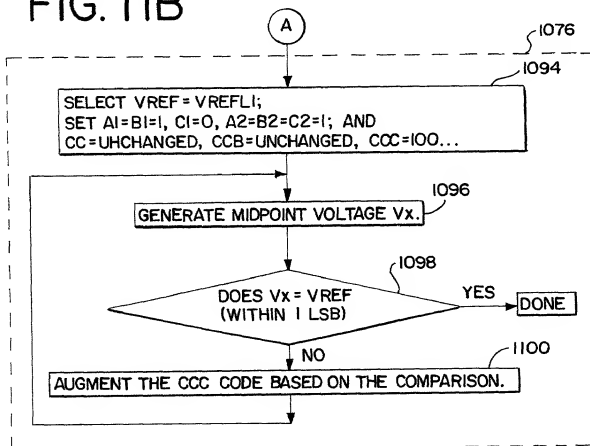


FIG. 11B



METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 12

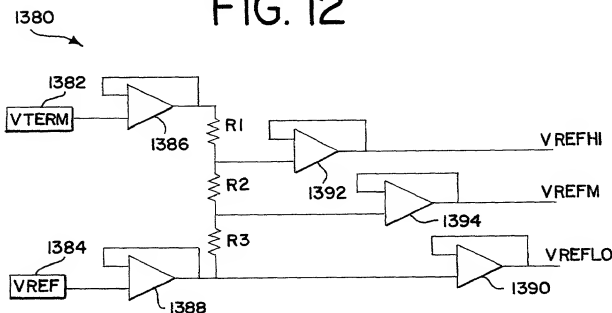
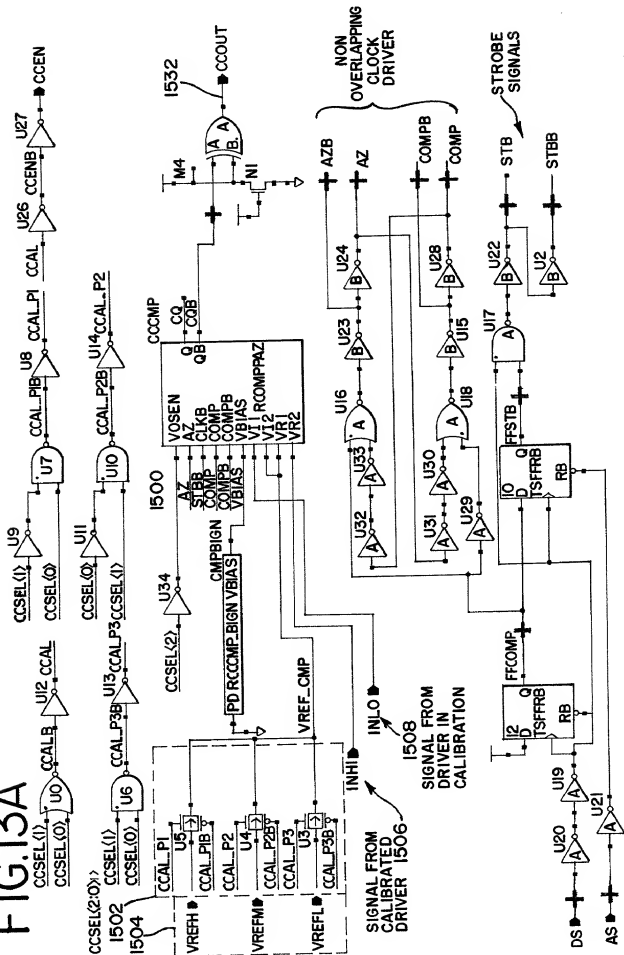
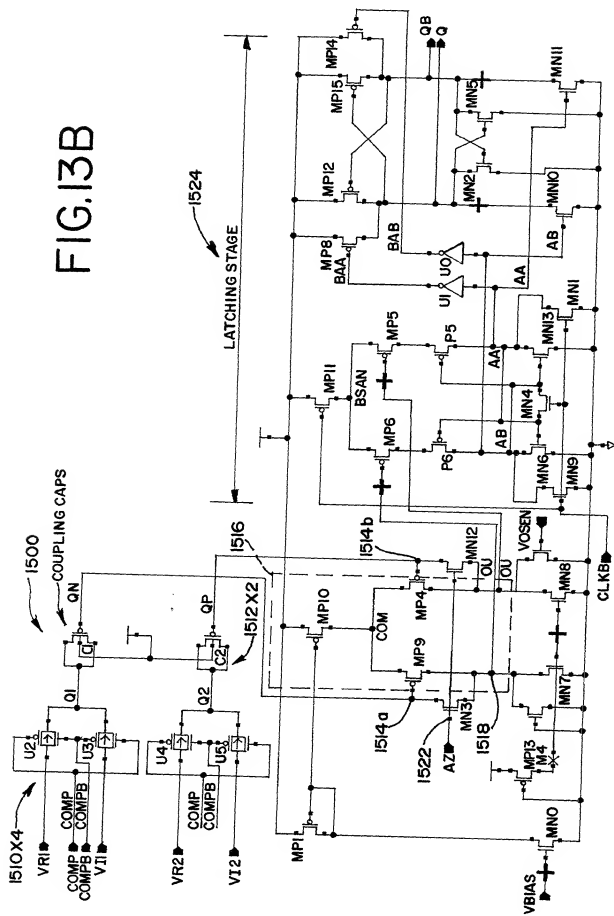


FIG. 13A



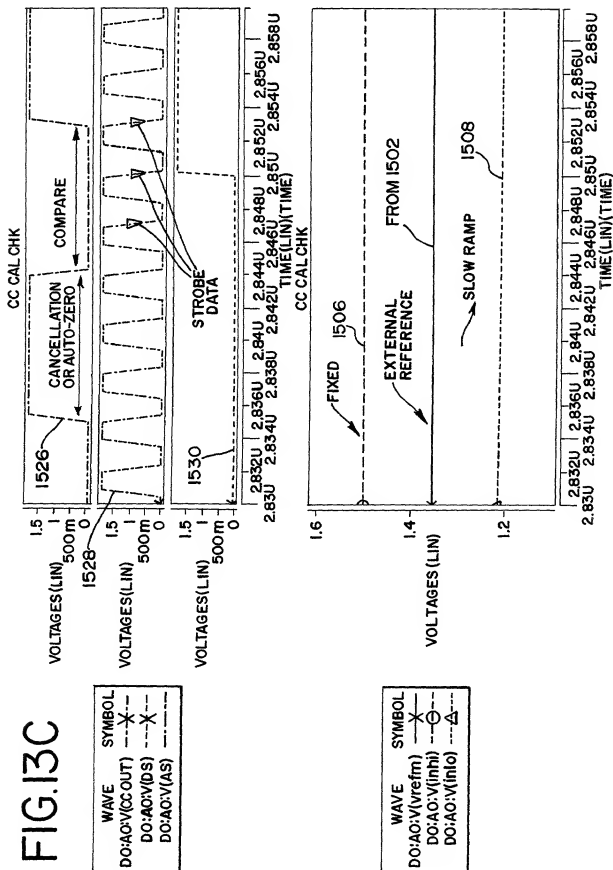
106280-0522h460

FIG.13B



FOE280-0522460

FIG.13C



106280-0522460

FIG. 13D

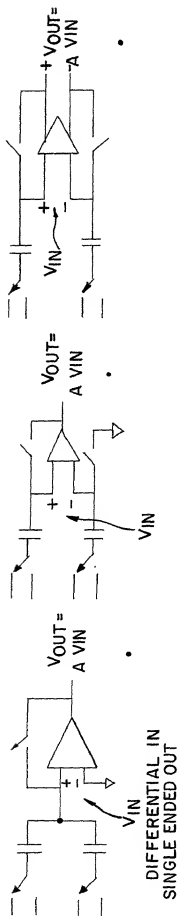
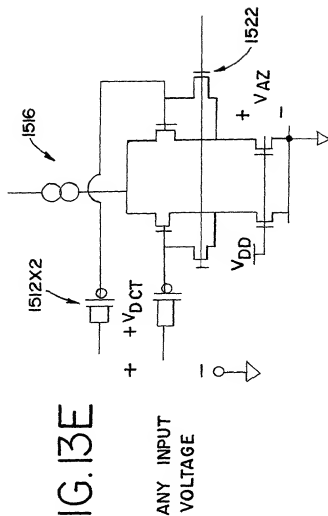


FIG. 13E



NON CCCAL MODE



NOTE: PLACE RI-8 AS FOLLOWING:
R6 R4 R3 R8
R5 R1 R2 R7
WHERE R5-8 ARE DUMMIES

LATCHING STAGE



The timing diagram displays several digital signals over a time interval from 13.98μs to 14.16μs. The signals are:

- CC CAL CHK:** A square wave alternating between logic 0 and 1.
- MISMATCH W/O S CANCELLATION:** A square wave that transitions at approximately 14.04μs and 14.10μs.
- CANCELLATION PHASE:** Indicated by a double-headed arrow spanning the period where MISMATCH W/O S CANCELLATION is high.
- CHK_OSC_MIS_OUB.XP EVB:** A square wave alternating between logic 0 and 1.
- CHK_OSC_MIS_OUB.XP EVB2:** A square wave alternating between logic 0 and 1.
- CHK_OSC_MIS_OUB.XP EVB6:** A square wave alternating between logic 0 and 1.
- CHK_OSC_MIS_OUB.XP VREF CMP:** A square wave alternating between logic 0 and 1.
- V.CMP:** A square wave alternating between logic 0 and 1.
- CHK_OSC_MIS_OUB.XP OU OUB:** A square wave alternating between logic 0 and 1.

The vertical axis represents voltage levels, with values ranging from 1.40 to 2.00. The horizontal axis represents time in microseconds (μs).

10E280*0522h460

FIG.14D

W/OS CANCEL

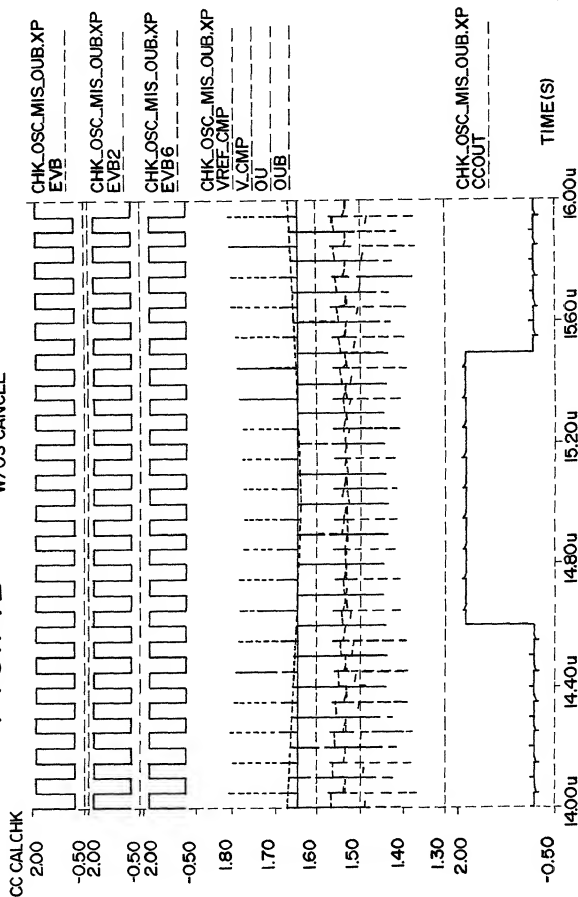


FIG.15A

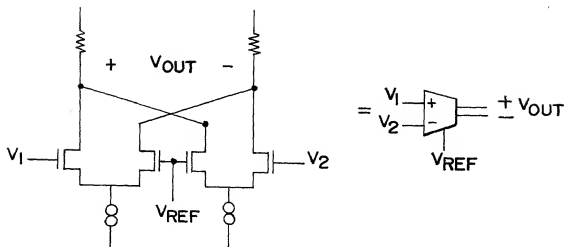


FIG.15B

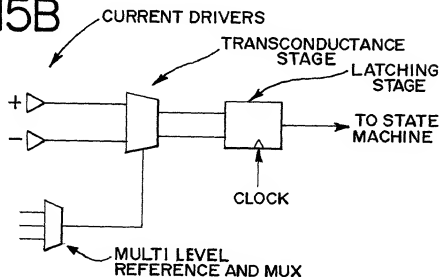


FIG.16

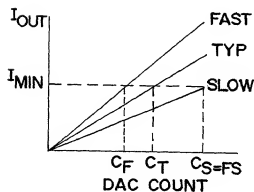


FIG.17

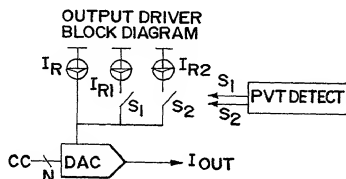


FIG. 18

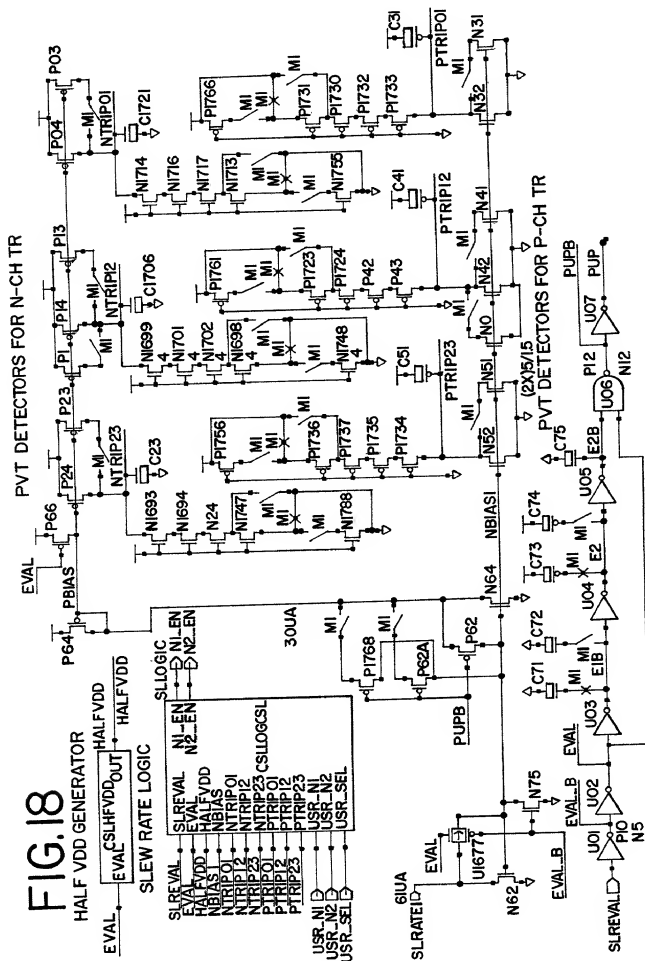


FIG.19A

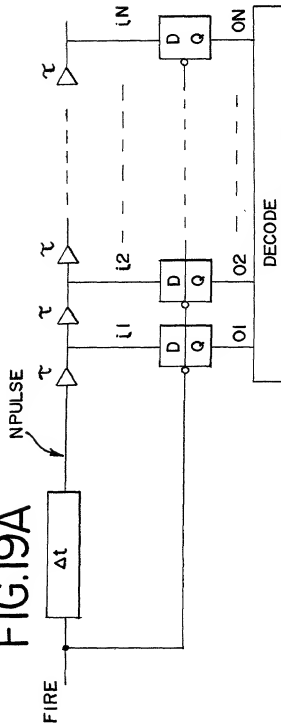


FIG.19B

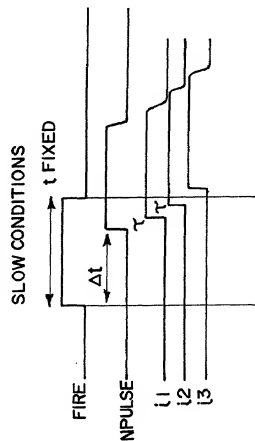
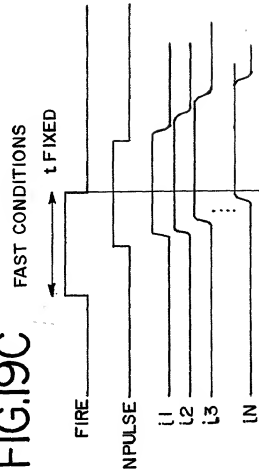
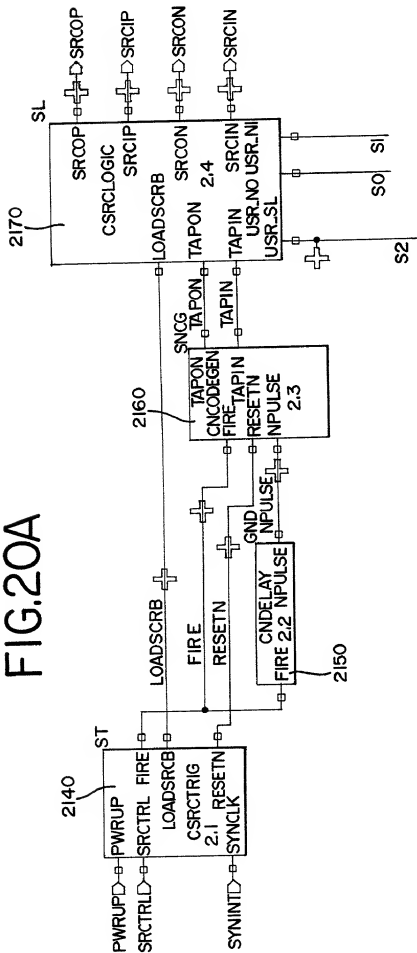


FIG.19C



106280-05224760

FIG. 20A



SO
SI
SZ

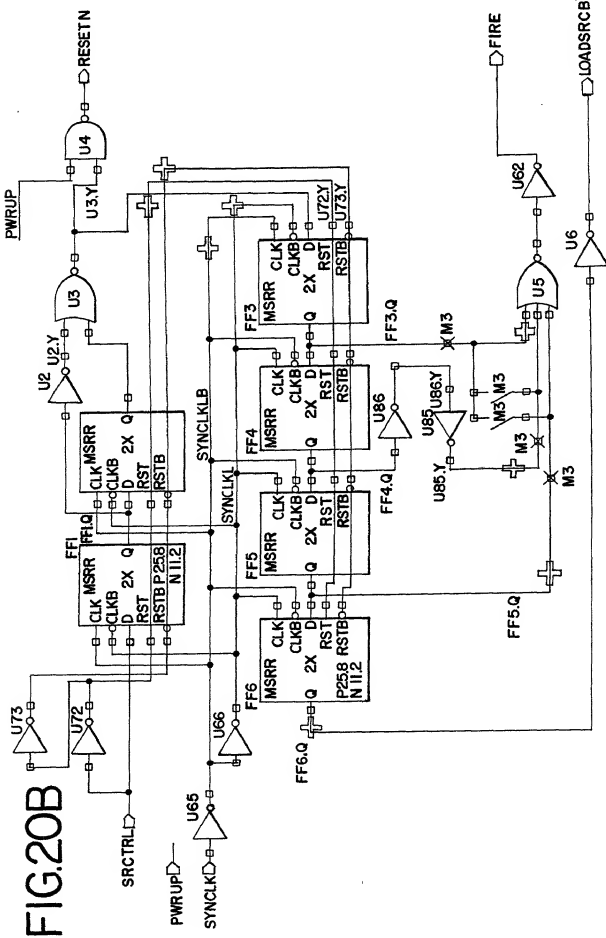
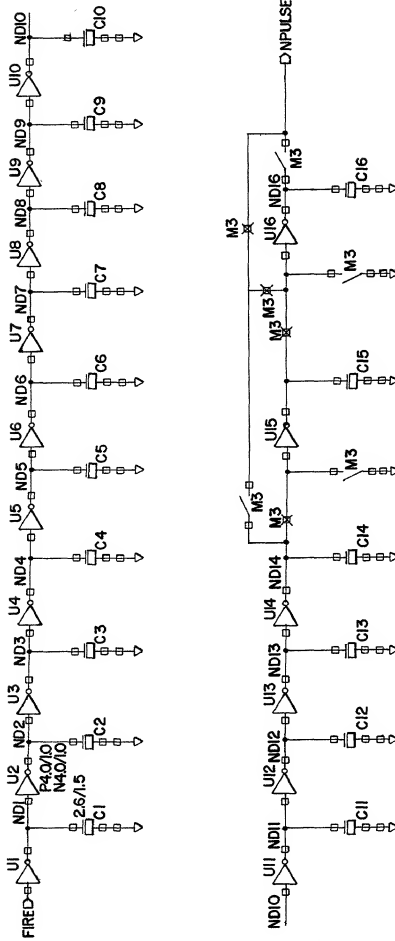


FIG. 20B

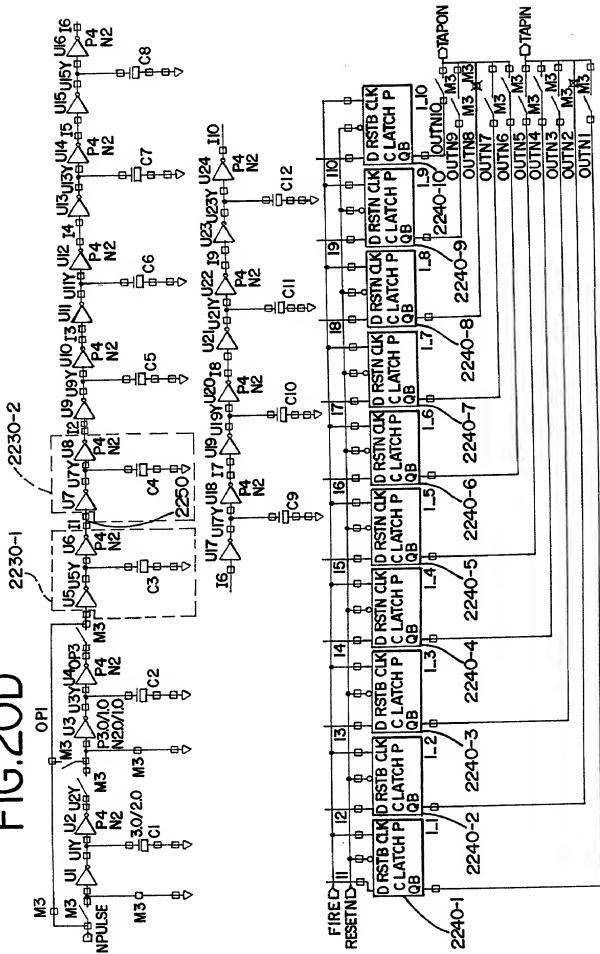
106280-05224760

FIG.20C



1062280-05224160

FIG.20D



10E280* 05224260

FIG.20E

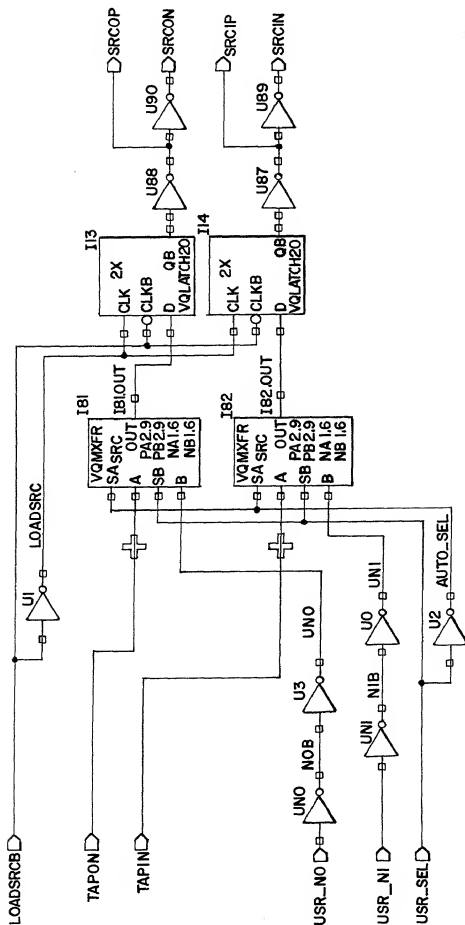


FIG. 20E

The schematic diagram shows a differential pair of transistors. The left transistor's gate is connected to a common-mode input signal V_{CM} . The right transistor's gate is connected to an input signal V_{IN} . The sources of both transistors are connected to a common source node, which is biased by a current source labeled 2310. The drain of the right transistor is connected to a node labeled 2320, which is also the input to a buffer labeled IX. The output of the buffer is V_{OUT} . The label 'I' is placed near the current source 2310.

FIG. 24A

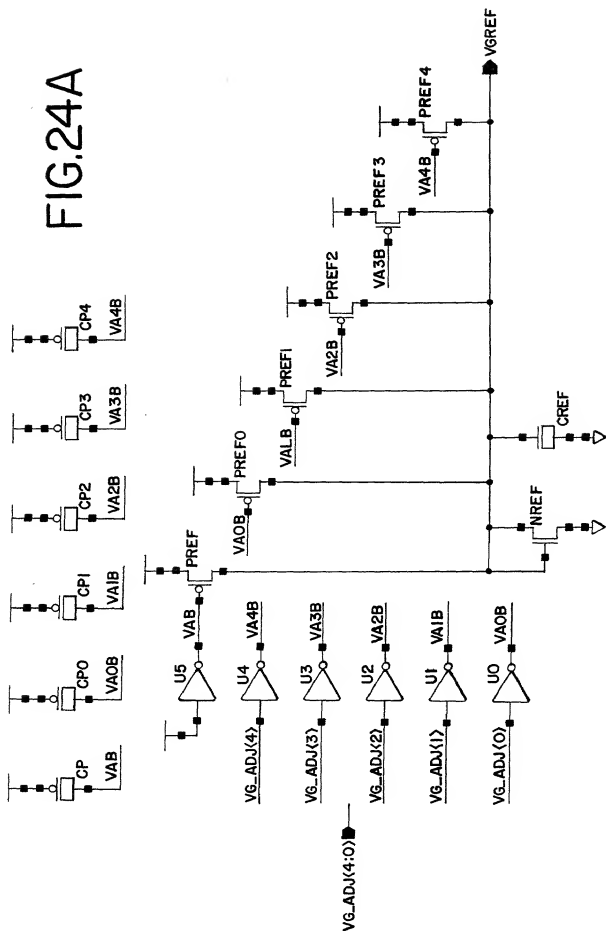


FIG.24B

